REPORT TO THE PRESIDENT

Revitalizing the U.S. Semiconductor Ecosystem

Executive Office of the President

President's Council of Advisors on Science and Technology

September 2022

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EXECUTIVE OFFICE OF THE PRESIDENT
PRESIDENT'S COUNCIL OF ADVISORS ON SCIENCE AND TECHNOLOGY
WASHINGTON, D.C. 20502

President Joseph R. Biden, Jr.
The White House
Washington, D.C.

September 20, 2022

Dear Mr. President:

Americans rely on semiconductors every day without even realizing it. They are used in mundane tasks—such as making a phone call, washing clothes, or taking public transportation—and in not-so-mundane tasks—such as providing the "intelligence" for smart weapons and autonomous surveillance. These tiny devices have become essential to every aspect of modern life, underpinning the global economy and our national security. Semiconductors are the fourth largest U.S. export, and the industry directly employs nearly 300,000 Americans and indirectly accounts for another 1.6 million jobs.

Since the 1940s, the federal government has played a central role in the development of the semiconductor industry through a strong partnership with industry and academia that has enabled the United States to become the world leader in semiconductor revenue. But that leadership position is being challenged like never before. The global share of semiconductors manufactured in the United States has declined from 37 percent in 1990 to just 12 percent today, and 90 percent of leading-edge semiconductor manufacturing is now done outside the United States, mostly in Asia.

You have been clear that maintaining our global leadership in semiconductors is a national priority to ensure both economic prosperity and national security. We agree. Without action, America stands to suffer lost jobs, stunted technological growth, considerable supply chain risk, and reduced economic opportunities.

The CHIPS and Science Act provides a once-in-a-generation opportunity to decisively strengthen the U.S. semiconductor ecosystem in the face of increasing global competition. By signing this bill into law, you have demonstrated the national commitment to sustain and grow our domestic semiconductor ecosystem and reap the benefits for the American people, including high-quality jobs, technological innovation, and scientific discovery. The federal government and private sector are poised to accelerate semiconductor manufacturing in the United States with a number of new projects ready to break ground.

Therefore, we have focused our report on the transformative investments in research and development (R&D), startups, education, and workforce development that are essential to the long-term health and competitiveness of the U.S. semiconductor ecosystem. We propose actions for maximally leveraging the historic $11 billion commitment appropriated for semiconductor R&D in the CHIPS and Science Act by:

- **Building a broad coalition**: We provide a framework for how the proposed National Semiconductor Technology Center should be structured to share the benefits of good jobs and educational opportunities across the United States.

- **Focusing on education and the future workforce**: We recommend that a portion of the funds go towards creating a national microelectronics training network.
- **Fostering innovation**: We recommend that a portion of the funds be used to provide startup companies and academic researchers with financial support and essential access to state-of-the art prototyping tools and facilities.
- **Setting a national research agenda**: We recommend setting national "grand challenges" to ensure that the United States leads the world in semiconductor innovation.

We are excited about the possibilities that the CHIPS and Science Act offers the American people in terms of economic potential and national security.

Sincerely,

Your President's Council of Advisors on Science and Technology

The President's Council of Advisors on Science and Technology

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Frances H. Arnold
Linus Pauling Professor of Chemical Engineering, Bioengineering, and Biochemistry
California Institute of Technology

Francis S. Collins
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The White House

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Senior Director, International Climate
Center for American Progress

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Bloomberg Distinguished Professor of Equity in Health and Healthcare and Director of the Center for Health Equity
Johns Hopkins University

John O. Dabiri
Centennial Professor of Aeronautics and Mechanical Engineering
California Institute of Technology

William Dally
Chief Scientist and Senior Vice President for Research
NVIDIA

Susan Desmond-Hellmann
Former CEO
Bill & Melinda Gates Foundation

Inez Fung
Professor of Atmospheric Science
University of California, Berkeley

Andrea Goldsmith
Dean of the School of Engineering and Applied Science and the Arthur LeGrand Doty Professor of Electrical and Computer Engineering
Princeton University

Laura H. Greene
Chief Scientist, National High Magnetic Field Laboratory
Florida State University, University of Florida, and Los Alamos National Laboratory
Marie Krafft Professor of Physics
Florida State University

Paula Hammond
Institute Professor, Head of the Department of Chemical Engineering, and member of the Koch Institute for Integrative Cancer Research
Massachusetts Institute of Technology

Eric Horvitz
Chief Scientific Officer
Microsoft

Joe Kiani
Chairman and CEO
Masimo

Jonathon Levin
Philip H. Knight Professor and Dean of the Graduate School of Business
Stanford University

Stephen Pacala
Frederick D. Petrie Professor in the Department of Ecology and Evolutionary Biology
Princeton University

Saul Perlmutter
Franklin W. and Karen Weber Dabby Professor of Physics and Director of the Berkeley Institute for Data Science
University of California, Berkeley
Senior Scientist
Lawrence Berkeley National Labs

William Press
Leslie Surginer Professor of Computer Science and Integrative Biology
The University of Texas at Austin

Penny Pritzker
Chairman
PSP Partners

Jennifer Richeson
Philip R. Allen Professor of Psychology and Director of the Social Perception and Communication Lab
Yale University

Vicki Sato
Professor of Management Practice (Retired)
Harvard Business School

Lisa Su
Chair and CEO
Advanced Micro Devices (AMD)

Kathryn D. Sullivan
Former NOAA Administrator
Former NASA Astronaut

Terence Tao
Professor & the James and Carol Collins Chair in the College of Letters and Sciences
University of California, Los Angeles

Philip Venables
Chief Information Security Officer
Google Cloud

Catherine Woteki
Visiting Distinguished Institute Professor in the Biocomplexity Institute
University of Virginia
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Iowa State University

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Principal Deputy Executive Director

Reba Bandyopadhyay
Deputy Executive Director

Kevin Johnstun
Research Analyst

Anne-Marie Mazza
Former Executive Director

Quinn Anex-Ries
Intern

Working Group on Semiconductors

Working Group members participated in the preparation of this report. The full membership of PCAST reviewed and approved the report.

Co-Leads

William Dally*
Chief Scientist and Senior Vice President for Research
NVIDIA

Lisa Su*
Chair and CEO
Advanced Micro Devices (AMD)

Members

Ahmad Bahai
Chief Technology Officer
Texas Instruments

Anantha Chandrakasan
Dean of the School of Engineering and Vannevar Bush Professor of Electrical Engineering and Computer Science
Massachusetts Institute of Technology

Scott J. DeBoer
Executive Vice President, Technology and Products
Micron Technology

Dario Gil
Senior Vice President
IBM

Andrea Goldsmith*
Dean of the School of Engineering and Applied Science and the Arthur LeGrand Doty Professor of Electrical and Computer Engineering
Princeton University

Ann Kelleher
Executive Vice President and General Manager of Technology Development
Intel

Tsu-Jae King Liu
Dean and Roy W. Carlson Professor of Engineering, College of Engineering and Distinguished Professor of Engineering and Computer Sciences
University of California, Berkeley

Priyanka Raina
Assistant Professor of Electrical Engineering
Stanford University

Pete Rodriguez
CEO
Silicon Catalyst

*Denotes PCAST Member

Executive Summary

Semiconductors are the foundation of today's information age and underpin the global economy. They are critical to U.S. economic and national security, and provide the "intelligence" behind data centers, communications, automotive, aerospace and defense, personal computing devices, industrial, entertainment, healthcare, and many other markets. To maintain global leadership from an economic and technological perspective, leadership in semiconductors is vital.

Currently, the United States is the global leader in semiconductor revenue, but that leadership is being challenged by global competitors like never before. For example, the global share of semiconductors manufactured in the United States has declined from 37 percent in 1990 to 12 percent today.[1] Meanwhile, countries in Asia, particularly China, have been investing heavily in semiconductor manufacturing and research and development (R&D) to grow their indigenous capabilities and bolster their presence in the global market.

For the United States to remain the world leader in the semiconductor industry, the majority of the *value added* in this industry must take place in the United States. PCAST enthusiastically supports the passage of the bipartisan CHIPS and Science Act, which includes significant funding for a once-in-a-generation opportunity to decisively strengthen the U.S. semiconductor ecosystem in the face of increasing global competition.[2] This investment demonstrates our national commitment to sustain and grow our domestic semiconductor ecosystem and reap the benefits for the American people, including high-quality jobs, technological innovation, and scientific discovery.

Industry and government efforts to support and accelerate semiconductor manufacturing are underway: a number of new projects are planned and ready to break ground as part of the Biden administration's efforts to expand semiconductor manufacturing in the United States.[3] However, the R&D initiatives—which are *equally* important to a strong and healthy U.S. semiconductor ecosystem—have not received nearly as much attention. To fill this gap, **this report provides recommendations for how the Biden administration can maximally leverage the semiconductor R&D funding in the CHIPS and Science Act to achieve the greatest benefits for the long-term health and competitiveness of the U.S. semiconductor ecosystem by creating a strong semiconductor R&D infrastructure, educating and training the next-generation semiconductor workforce, and driving our national research and innovation agenda.**

The CHIPS and Science Act provides funding for the Department of Commerce to invest $11 billion over 5 years in semiconductor R&D, including a National Semiconductor Technology Center (NSTC)

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[1] Semiconductor Industry Association. (2022). 2022 Factbook. https://www.semiconductors.org/wp-content/uploads/2022/05/SIA-2022-Factbook_May-2022.pdf

[2] Division A ("CHIPS Act of 2022") of Public Law 117-167 (commonly known, and referred to herein, as the "CHIPS and Science Act") appropriates funding for activities authorized in Title XCIX ("Creating Helpful Incentives to Produce Semiconductors (CHIPS) for America") of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021 (Pub. L. 116-283) (referred to herein as the "CHIPS for America Act").

[3] White House (2022, August 9). *CHIPS and Science Act will lower costs, create jobs, strengthen supply chains, and counter China [Fact sheet]*. https://www.whitehouse.gov/briefing-room/statements-releases/2022/08/09/fact-sheet-chips-and-science-act-will-lower-costs-create-jobs-strengthen-supply-chains-and-counter-china

and a National Advanced Packaging Manufacturing Program (NAPMP),[4] in addition to $39 billion the legislation appropriates for financial assistance for domestic semiconductor manufacturing. This is a historic and significant investment in semiconductor R&D that can decisively strengthen the U.S. semiconductor ecosystem. For this to happen, the NSTC and NAPMP must inspire broad collaboration between the public and private sectors, develop and grow the semiconductor talent in the United States, and drive an ambitious research and innovation agenda.

Implementation of the 10 recommendations outlined in this report will lay a strong foundation for revitalizing the U.S. semiconductor ecosystem. Each of these measures can be initiated by the Biden administration, using a comprehensive public-private partnership approach that will sustain and grow our domestic semiconductor ecosystem. We believe that the implementation of these initiatives can change our current trajectory and rebuild our global leadership in semiconductors.

Recommendations

1. The Secretary of Commerce should establish NSTC as an independent legal entity in public-private partnership by the end of 2023. The Secretary of Commerce should select a Board of Directors, and that Board should oversee both the NSTC and the NAPMP to ensure synergy and alignment in the investments. The Board members should include broad representation from government, industry, and academia.

2. The Secretary of Commerce should ensure that the NSTC founding charter includes establishing prototyping capabilities in a geographically distributed model encompassing up to six coalitions of excellence (COEs) aligned around major technical thrusts such as advanced logic; advanced memory; analog and mixed-signal; life science applications; design and methodologies; and packaging. The packaging COE should encompass the budget and the objectives of the NAPMP initiatives.

3. The Secretary of Commerce in coordination with the Director of the National Science Foundation (NSF) should support the establishment of a national microelectronics education and training network by the end of 2023 and allocate funding on the order of $1 billion over the next 5 years to upgrade educational laboratory facilities, support curriculum development, and facilitate hiring of faculty into this field.

4. The Secretary of Commerce should ensure that NSTC-funded research (from Recommendation 8, below) supports on the order of 2,500 scholarships and research assistantships per year across the educational spectrum.

5. The Department of Homeland Security should implement existing statutory and regulatory authorities to provide premium processing to newly filed Immigrant Petitions for employment-based second preference advanced degree immigrants seeking a National Interest Waiver to work in microelectronics endeavors.

6. The Secretary of Commerce should ensure that by the end of 2023, the NSTC creates an investment fund on the order of $500 million to provide financial support and in-kind access to prototyping and tools for semiconductor startups.

[4] Appropriations in CHIPS and Science Act § 102; authorizations in CHIPS for America Act § 9906(c) for the NSTC and § 9906(d) for the NAPMP.

7. The Secretary of Commerce should ensure that the NSTC creates or funds the creation of a "chiplet" platform[5] with a complete software stack by the end of 2025 so that startups and academic institutions can integrate their custom chiplet(s) with the NSTC-supported chiplet platform to demonstrate new innovations with dramatically reduced investment and time.

8. The Secretary of Commerce should ensure that the NSTC founding charter allocates a significant portion of the annual funding, on the order of 30 to 50 percent, to directly fund a national research agenda. This research agenda should be broad in nature and address the following areas: materials, process, and manufacturing technologies; packaging and interconnect technologies; energy-efficient computing and domain-specific accelerators; design automation tools and methods; semiconductor and system security; and semiconductors and life sciences.

9. The NSTC should identify a set of nationwide grand challenges that are enabled through collaboration across the NSTC industrial membership and NSTC-funded research. These grand challenges should span three complementary areas that would benefit from large-scale nationwide collaboration: advanced computing into the zettascale[6] era; significantly reducing design complexity; and proliferating semiconductors in life sciences applications.

10. To improve visibility into federal semiconductor investment efforts, measure the progress across the industry at the federal level, and maximize the leverage of such investments, we recommend the following:

    a) Starting in 2023, and annually thereafter, the Networking and Information Technology Research and Development (NITRD) program should collate and publish annual investment figures for semiconductors across all federal agencies.

    b) The NSTC should encourage all agencies with semiconductor R&D investments to leverage and utilize the NSTC facilities and capabilities. We recommend the NSTC expand and co-fund programs with other agencies and in public-private partnership where the research agendas are synergistic including, for example, Defense Advanced Research Projects Agency's (DARPA's) Electronics Resurgence Initiative, Research on the Future of Semiconductors sponsored by the Computer and Information Science and Engineering Directorate at NSF, and the broad multi-sector collaborations enabled by the Semiconductor Research Corporation.

    c) The Secretary of Commerce should develop and regularly evaluate performance measures to assess progress, effectiveness, outcomes, and impact of the CHIPS and Science Act initiatives and report them annually to the President.

[5] A chiplet platform is an integrated circuit that is composed of multiple smaller chips where the common, non-innovative parts of a product have been specifically designed so that customizable components ("chiplets") can be added to address particular applications, performance, or functionality.
[6] 1 zettaflop = 10^3 exaflops = 10^{21} floating point operations per second.

Revitalizing the U.S. Semiconductor Ecosystem

State of the Semiconductor Ecosystem

Semiconductors are essential to every aspect of modern life—enabling work, study, commerce, communication, transportation, aerospace, defense, healthcare, and many other industries. Since the 1940s, the federal government has played a central role in the development of the semiconductor industry through a deep partnership with industry and academia that has enabled the United States to become the world leader in semiconductors in terms of revenue. Analyses by the Semiconductor Industry Association found that global semiconductor revenues are $556 billion,[7] with U.S. companies accounting for 47 percent of the market; semiconductors are the fourth largest U.S. export; and the industry directly employs nearly 300,000 Americans and indirectly accounts for 1.6 million additional jobs.[8] Not only are semiconductors critical to our economic strength, but they also are key to our national security. Semiconductors provide the "intelligence" for smart weapons and precision-guided munitions, and they are required components of almost all military systems. Supercomputers based on semiconductors are used for cryptanalysis, to design weapons systems, and to ensure the safety and reliability of the nuclear stockpile. As such, our national defense depends on our global leadership in the design and development of microelectronic systems and the skilled semiconductor workforce that carries out this important work.

The COVID-19 pandemic led to an unprecedented increase in demand for products that rely on semiconductors, resulting in supply chain disruptions that highlighted both the critical importance of semiconductors and the fragility of the semiconductor ecosystem.[9] It has never been clearer that leadership in semiconductors is a national priority to ensure both our economic prosperity and our national security.

Although U.S.-headquartered companies lead the world in revenue, our leadership in semiconductors has been declining in recent years, while Asia's capabilities have been increasing. Recognizing the strategic importance of semiconductors, many governments in Asia have invested significantly through industrial policy to grow their footprint and capabilities. For example, South Korea's semiconductor revenue has grown rapidly in recent years and now stands at 21 percent of the global market, driven by their technological advances in memory and storage.[10] Taiwan is now the powerhouse in manufacturing, producing 92 percent of the world's leading-edge semiconductors.[11] In June 2014, the Chinese government published an ambitious plan committing $150 billion over 10 years to advance semiconductor research, development, and manufacturing, with the goal of

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[7] Semiconductor Industry Association. (2022). 2022 Factbook. https://www.semiconductors.org/wp-content/uploads/2022/05/SIA-2022-Factbook_May-2022.pdf

[8] Semiconductor Industry Association. (2021) State of the U.S. Semiconductor Industry. https://www.semiconductors.org/wp-content/uploads/2021/09/2021-SIA-State-of-the-Industry-Report.pdf

[9] Hsu, J. (2021, June 30). The great chip crisis threatens the promise of Moore's law. *MIT Technology Review*. https://www.technologyreview.com/2021/06/30/1026438/global-microchip-shortage-problem-m1-apple-tsmc-intel

[10] Semiconductor Industry Association. (2022). 2022 Factbook. https://www.semiconductors.org/wp-content/uploads/2022/05/SIA-2022-Factbook_May-2022.pdf

[11] White House. (2021). *Building resilient supply chains, revitalizing American manufacturing, and fostering broad-based growth: 100-day review under Executive Order 14017*. https://www.whitehouse.gov/wp-content/uploads/2021/06/100-day-supply-chain-review-report.pdf

becoming the world leader in semiconductors by 2030. In 2019, China announced the creation of a second semiconductor fund committed to invest an additional $29 billion.[12] Recently, large investments have also been announced by South Korea[13] and the European Union.[14]

Today, about 12 percent of semiconductors are manufactured in the United States, continuing a long-term decline from 37 percent in 1990.[15] In 2021, 85 percent of semiconductor fabrication equipment was destined for countries in Asia (28 percent of that going to China), while only 7 percent of fabrication equipment was destined for use in North America.[16] If the United States does not increase investments in semiconductor manufacturing, it is estimated that our nation will be on a path to manufacturing less than 10 percent of the world's semiconductors by 2030, while China will be manufacturing nearly 30 percent of the global supply.[17]

Startups have been a key driver of the semiconductor industry's success since its inception. However, the funding of semiconductor startups in the United States has not kept pace with other countries. New venture funding reported for the month of May 2022[18] showed that only 18 percent of funded semiconductor startups were based in the United States, compared to 59 percent based in China.[19] Relatedly, the rate and pace of U.S. federal funding for semiconductor-related research and development (R&D) activities has been relatively flat as a percentage of gross domestic product, while the scale of investment required for success in this area has increased dramatically.[20]

In January 2017, PCAST issued a report to President Obama identifying actions to ensure long-term U.S. leadership in the global semiconductor ecosystem.[21] The core finding of that report was that the United States could only retain leadership by *innovating* and running *faster*. This remains the case today and the need for action has become even more urgent.

To reverse the decline in U.S. semiconductor leadership, the Biden administration has taken bold action to invest in, develop, and implement a comprehensive strategy that rebuilds the domestic semiconductor ecosystem and strengthens U.S. leadership in the face of increasing global competition. The bipartisan Creating Helpful Incentives in Producing Semiconductors (CHIPS) for

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[12] Sutter, K. (2021). *China's new semiconductor policies: Issues for congress* (CRS Report No. R46767) Congressional Research Service. https://crsreports.congress.gov/product/pdf/R/R46767

[13] Jaewon, K. (2021, May 13) South Korea plans to invest $450 bn to become chip 'powerhouse.' NikkeiAsia. https://asia.nikkei.com/Business/Tech/Semiconductors/South-Korea-plans-to-invest-450bn-to-become-chip-powerhouse

[14] European Commission. (2022, February 8). Digital sovereignty: Commission proposes Chips Act to confront semiconductor shortages and strengthen Europe's technological leadership [Press release]. https://ec.europa.eu/commission/presscorner/detail/en/ip_22_729

[15] Semiconductor Industry Association. (2022). 2022 Factbook. https://www.semiconductors.org/wp-content/uploads/2022/05/SIA-2022-Factbook_May-2022.pdf

[16] Patel, D. (2022, June 13). Why America will lose semiconductors. *SemiAnalysis*. https://semianalysis.substack.com/p/why-america-will-lose-semiconductors

[17] https://semianalysis.substack.com/p/why-america-will-lose-semiconductors

[18] Patel 2022 notes that other months showed a similar trend.

[19] Patel, D. (2022, June 13). Why America will lose semiconductors. *SemiAnalysis*. https://semianalysis.substack.com/p/why-america-will-lose-semiconductors

[20] Semiconductor Industry Association. (2020). *Sparking Innovation: How federal investment in semiconductor R&D spurs U.S. economic growth and job creation*. https://www.semiconductors.org/wp-content/uploads/2020/06/SIA_Sparking-Innovation2020.pdf

[21] PCAST. (2017). Report to the President: Ensuring long-term U.S. leadership in Semiconductors. https://obamawhitehouse.archives.gov/sites/default/files/microsites/ostp/PCAST/pcast_ensuring_long-term_us_leadership_in_semiconductors.pdf

America Act was enacted into law in January 2021 as part of the National Defense Authorization Act for Fiscal Year 2021.[22] Subsequently, on August 9, 2022, President Biden signed into law the CHIPS and Science Act, which appropriated $50.7 billion for investment in semiconductors, including incentives to support U.S. manufacturing and investments in semiconductor R&D authorized in the CHIPS for America Act.[23]

The CHIPS and Science Act is a historic and game-changing investment that has the potential to reverse the downward trajectory of our nation's position in the global semiconductor ecosystem, providing us with a once-in-a-generation opportunity to ensure that the United States is the clear leader in semiconductors for decades to come. To supplement the efforts to boost semiconductor manufacturing, which have been well-covered by industry and federal government efforts, this report provides recommendations for how the Biden administration can maximally leverage implementation of the $11 billion in R&D investments appropriated in this Act across the U.S. semiconductor ecosystem for the benefit of our economic and national security.

Formation of the National Semiconductor Technology Center (NSTC)

Over the last two decades, semiconductor technology has become increasingly complex, requiring substantially more investment to develop next-generation technologies. The costs for semiconductor development now approach hundreds of millions of dollars for design at the leading-edge of technology and an investment of billions of dollars for prototyping and manufacturing.[24] Because of these high costs, fewer companies and academic institutions can afford to participate in R&D, which has serious implications for the future of semiconductor innovation in the United States.

This problem can be addressed with the creation of a national R&D infrastructure that companies and academia can share.[25] Without shared infrastructure, most companies, researchers, and entrepreneurs will continue to face significant, if not insurmountable, barriers to innovation. The CHIPS and Science Act provides funding for the Department of Commerce to create a National Semiconductor Technology Center (NSTC) and a National Advanced Packaging Manufacturing Program (NAPMP) that will provide the shared infrastructure needed to support and bolster semiconductor R&D in the United States.[26] The NSTC will establish leading-edge semiconductor and packaging prototyping facilities that can be used by academia, startups, and established companies. This center will enable fast, low-cost prototyping in a shared environment while advancing the U.S. agenda in research and accelerating semiconductor workforce development. In conjunction with the NSTC, the NAPMP will establish a national program to strengthen semiconductor advanced test, assembly, and packaging capabilities in the United States. This infrastructure will enable the demonstration of new innovations without requiring significant investment in facilities by individual

[22] Title XCIX ("Creating Helpful Incentives to Produce Semiconductors (CHIPS) for America") of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021 (Pub. L. 116-283).
[23] Division A ("CHIPS Act of 2022") of Public Law 117-167 (commonly known as the "CHIPS and Science Act").
[24] Bauer, H., Burkacky, O., Lingemann, S., Pototzky, K., Kenevan, P., & Wiseman, B. (2020, August 20). *Semiconductor design and manufacturing: Achieving leading-edge capabilities.* McKinsey and Company. https://www.mckinsey.com/industries/advanced-electronics/our-insights/semiconductor-design-and-manufacturing-achieving-leading-edge-capabilities
[25] The research and development work envisioned as part of the NSTC would be considered pre-competitive in nature, and thus allow companies and academia to collaborate on common solutions.
[26] Appropriations in CHIPS and Science Act § 102; authorizations in CHIPS for America Act § 9906(c) for the NSTC and § 9906(d) for the NAPMP.

institutions or the long lead times that are currently needed. We strongly support these initiatives and provide recommendations for their structure, governance, and implementation.

Recommendation 1: The Secretary of Commerce should establish NSTC as an independent legal entity in public-private partnership by the end of 2023. The Secretary of Commerce should select a Board of Directors, and that Board should oversee both the NSTC and the NAPMP to ensure synergy and alignment in the investments. The Board members should include broad representation from government, industry, and academia.

The NSTC is the largest undertaking of its kind in U.S. semiconductor history. The only similar venture, SEMATECH, a public-private partnership formed in 1987 between U.S. semiconductor firms and the Defense Advanced Research Projects Agency (DARPA), began on a much smaller scale with a $500 million initial investment.[27]

Successful execution of the NSTC will require the right structure, governance, and guiding principles. PCAST recommends that the NSTC should be established as a public-private partnership to foster participation, collaboration, and innovation across the entire U.S. semiconductor ecosystem. The Department of Commerce should encourage broad academic, industry, and government participation in the NSTC. Industry participation should span all aspects of the semiconductor ecosystem including materials and equipment suppliers, electronic design automation companies, fabless design companies, integrated device manufacturers, foundries, and system companies. Federal government participation should include agencies with deep domain expertise in semiconductors, for example the National Science Foundation (NSF) and DARPA, among others.

The Secretary of Commerce should merge the governance of the NSTC and the NAPMP to increase the synergy of investment and reduce the potential for duplication of infrastructure. The Board of Directors overseeing both initiatives should be comprised of members from the U.S. semiconductor industry along with representation from academia and the U.S. government. The Board should select an independent NSTC chief executive officer (CEO) and create a Technology Advisory Council to guide the research agenda. The NAPMP can be managed as a distinct entity within the NSTC with its own budget while contributing to and participating in the larger NSTC research agenda. Figure 1 illustrates a proposed NSTC governance and operating model.

The NSTC should collaborate, where possible, with similar organizations outside the United States (e.g., Europe's Interuniversity Microelectronics Centre and semiconductor companies from allied countries) to leverage resources, existing infrastructure, and capabilities. Such engagements should reflect principles of reciprocity, research security, and alignment to shared values. However, due to the strategic nature of this effort from a global competition and national security standpoint, no foreign entities should be members of the Board of Directors or the Technology Advisory Council.

[27] Wells Jr., J. E., Mininger, L., Cheston, R., Quicksal, J., Viola J., & Russell, C. B. (1992). *Federal research: Lessons learned from SEMATECH.* Government Accountability Office. https://www.gao.gov/assets/rced-92-283.pdf

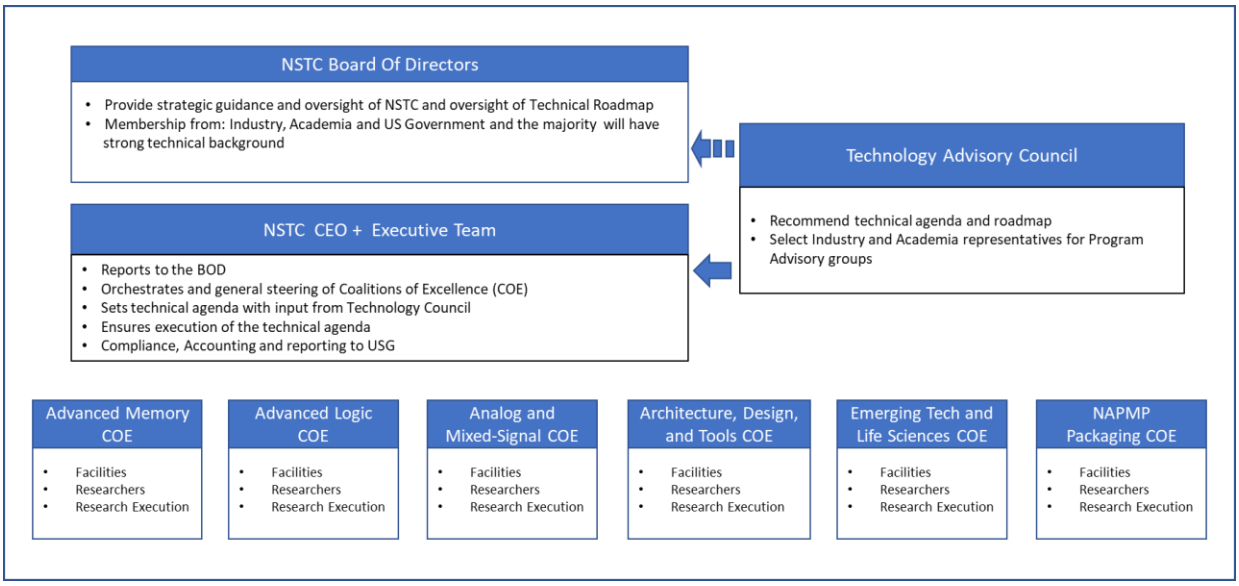

Figure 1: NSTC proposed structure

Recommendation 2: The Secretary of Commerce should ensure the NSTC founding charter includes establishing prototyping capabilities in a geographically distributed model encompassing up to six coalitions of excellence (COEs) aligned around major technical thrusts such as advanced logic; advanced memory; analog and mixed-signal; life science applications; design and methodologies; and packaging. The packaging COE should encompass the budget and the objectives of the NAPMP initiatives.

Unlike previous efforts, such as SEMATECH, where there was one central location for the infrastructure, we believe the NSTC infrastructure should be built in a distributed regional model given the breadth of technologies to be covered. This will also distribute the job creation opportunities across the nation. NSTC should be linked to academic institutions to support education and workforce development, as well as providing facilities for conducting academic research.

To achieve these results, the NSTC prototyping infrastructure should leverage current ecosystems and infrastructure wherever possible, augmenting regional and academic infrastructure, as necessary. As one model, the NSTC could organize around six COEs that include broad academic, industry, and regional representation: 1) advanced memory; 2) advanced logic; 3) analog and mixed-signal; 4) architecture, design and tools; 5) packaging (including the mission of the NAPMP initiative); and 6) emerging technologies including life sciences. These six thrusts represent the key technologies that are required for a strong and vibrant U.S. semiconductor ecosystem.

Each COE should be highly multi-disciplinary and cross-functional in nature, with prototyping capabilities and a research agenda that covers materials, devices, equipment, modeling, testing, and other disciplines. The prototyping capabilities of each COE should support academic, startup, and industry activities. Strong coordination amongst the COEs will be essential to deliver integrated systems and solutions that support the research agenda and the grand challenges that are outlined in Recommendations 8 and 9. There is also an opportunity to leverage the NSTC infrastructure together with other federal initiatives, such as the Department of Defense's Microelectronics

Commons,[28] which aims to provide "lab to fab" prototyping capabilities to strengthen defense-related microelectronics innovation in the United States. Examples of COE activities are provided in Box 1.

Box 1: Examples of Coalitions of Excellence Activities

The analog and mixed-signal COE could have research and prototyping capabilities for next generation analog, mixed-signal, power management and high-voltage devices, radio frequency and high-speed technologies, and intelligent sensing. These activities could support a broad range of academic and commercial applications in communications infrastructure, smart cities, autonomous vehicles, green energy, along with medicine, health care, and wellness.

The advanced logic COE could have research and prototyping capabilities for next generation advanced logic, memory, chiplets, and 3D and heterogeneous integration. The advanced memory COE could focus on research and prototyping capability for future generations of memory, new memory technology concepts, and heterogeneous integration of memory with compute and advanced 3D memory concepts. These two COE activities would support a broad range of academic and commercial applications to enable leadership in leading-edge semiconductor process technology and products. They also would work closely with the packaging COE in areas that relate to 2.5D/3D packaging and heterogeneous integration.

A robust intellectual property (IP) framework—including patents, trademarks, copyrights, and trade secrets—is critical to maintaining U.S. semiconductor leadership and to the NSTC's long term success. The IP framework for ownership and licensing is also critical for lowering the barrier to entry for startups and academic researchers and for shortening the time needed to go from "lab to fab" through access to enabling IP. We recommend that all IP developed with funding by a COE (i.e., membership fees, government funding, state or university funding) be licensed to COE members in good standing as a non-exclusive, royalty-free perpetual license for research and commercial products. Ownership of IP will be retained by the inventors or inventors' respective institutions. Any pre-existing IP which is necessary to practice the IP created by the NSTC will be identified up front by the owner of the pre-existing IP. If the NSTC chooses to use this pre-existing IP, it should be licensed to members on the best terms possible. Best practices from established research models, such as Semiconductor Research Corporation and Europe's Interuniversity Microelectronics Centre, should be applied in the final IP framework and security definition.

Education and Workforce Development

The complexity and sophistication of semiconductor integrated circuit "chip" design and manufacturing require a highly trained microelectronics workforce with knowledge and skills spanning a wide range of science, technology, engineering, and math (STEM) disciplines and educational levels. More than 50 percent of workers in the semiconductor industry have a bachelor's

[28] For more information, see https://www.cto.mil/ct/microelectronics.

or graduate degree.[29] In addition, the remainder of the jobs associated with the semiconductor industry are good paying jobs that require a skilled technical workforce. A study from the Semiconductor Industry Association[30] estimates that the Chips and Science Act's manufacturing incentives will create an extra 280,000 new jobs in the United States over the next few years, with 42,000 directly created in the semiconductor industry, 101,000 created to support the supply chain, and the remaining jobs created through wage spending.[31] Many of these new jobs will be concentrated in high-skilled engineering and technician roles, but U.S. universities, colleges, and trade schools presently do not graduate anywhere near the number of students required to meet this demand.

To attract significantly more students to the study of semiconductors, coursework must capture their interests and imagination. To do this, it is important to empower small groups of students to innovate and get hands-on experience building their own semiconductor chips. This is not possible with today's chip design approach due to the long times required to build hardware and the overall complexity of the chip design and prototyping process. The ability for small teams to rapidly demonstrate ideas is what drove the semiconductor revolution in the 1980s and is a key force pulling students into computer science today. Therefore, there is an urgent need to reinvigorate student interest in semiconductors by creating motivating course experiences and providing opportunities for hands-on chip design and prototyping. This requires updating educational curricula and academic research and training facilities to keep pace with advances in chip design and manufacturing technology. There is also an urgent need to provide students with practical work experience through paid internships and apprenticeships.

Recommendation 3: The Secretary of Commerce in coordination with the Director of NSF should support the establishment of a national microelectronics education and training network by the end of 2023 and allocate funding on the order of $1 billion over the next 5 years to upgrade educational laboratory facilities, support curriculum development, and facilitate hiring of faculty into this field.

To ensure that the U.S. microelectronics ecosystem has a healthy pipeline of talent to thrive and to retain global leadership in semiconductor research, design, and manufacturing, new approaches are needed to attract and train a much larger and more diverse workforce. A survey from 2021 found that Black employees comprised 4 percent and Hispanic employees comprised 13 percent of the semiconductor workforce, which lags behind both the manufacturing sector and the American

[29] Semiconductor Industry Association and Oxford Economics. (2021) *Chipping in: The positive impact of the semiconductor industry on the American workforce and how federal industry incentives will increase domestic jobs.* https://www.semiconductors.org/wp-content/uploads/2021/05/SIA-Impact_May2021-FINAL-May-19-2021_2.pdf

[30] Semiconductor Industry Association and Oxford Economics. (2021) *Chipping in: The positive impact of the semiconductor industry on the American workforce and how federal industry incentives will increase domestic jobs*. https://www.semiconductors.org/wp-content/uploads/2021/05/SIA-Impact_May2021-FINAL-May-19-2021_2.pdf

[31] These new jobs would be in addition to the jobs that would be created without the new investments from the CHIPS and Science Act.

workforce as a whole.[32,33] Additionally, as of 2019, less than 25 percent of employees in the semiconductor workforce were women, and less than 1 percent of leadership roles at the majority of semiconductor companies were held by women.[34] As we look to grow the overall number of workers in the semiconductor field, we must draw on *all* of the nation's talent, from *all* backgrounds and geographic regions. In order to have a broad and diverse workforce, we have to reach students where they are. Talented students are located all over the country, and they are at all types of institutions. Explicit efforts must be made to create opportunities for all students and workers, especially those who have historically been underserved in terms of STEM and microelectronics education, and provide access to good-paying jobs across the country. Toward this end, the national microelectronics training network should include upgrading laboratory facilities and equipment for at least 50 "hub" universities and colleges geographically distributed across the country, including minority serving institutions (e.g., Historically Black Colleges and Universities, Hispanic Serving Institutions, Asian American and Pacific Islander Serving Institutions, and Tribal Colleges and Universities); curriculum development and dissemination to universities, community colleges, and trade schools; and hiring of new microelectronics faculty at academic institutions across the nation.

Specific recommendations to reinvigorate microelectronics education and support workforce development across the United States are provided in Box 2.

[32] Semiconductor Industry Association and Oxford Economics. (2021) *Chipping in: The positive impact of the semiconductor industry on the American workforce and how federal industry incentives will increase domestic jobs*. https://www.semiconductors.org/wp-content/uploads/2021/05/SIA-Impact_May2021-FINAL-May-19-2021_2.pdf

[33] U.S. Bureau of Labor Statistics. (2021) *Labor force characteristics by race and ethnicity, 2020*. https://www.bls.gov/opub/reports/race-and-ethnicity/2020/home.htm

[34] GSA & Accenture. (2020). *GSA: Women in the Semiconductor Industry [2019 Survey Brief Results].* GSA Women's Leadership Initiative. https://www.gsaglobal.org/wp-content/uploads/2020/05/BRIEF-GSA-Women-in-the-Semiconductor-Industry-Survey-Results-2019.pdf

Box 2: Recommendations to Reinvigorate Microelectronics Education and Support Workforce Development Across the United States

1. **$750 million over 5 years ($150 million per year)** to upgrade existing educational and research laboratory facilities and equipment critical for hands-on learning and training in semiconductor design, manufacturing, packaging and testing, and to cover operational costs of hands-on learning and training programs in the laboratories at the 50 hub academic institutions.

2. **$100 million over 5 years ($20 million per year)** to support curriculum development and sharing across the nationwide network of academic institutions including universities, community colleges, and trade schools. The university curriculum would include courses on chip design and prototyping of student-designed chips, while the community college and trade school curriculum would include technical training. A few universities within the network would be funded to maintain the software tools and flows for chip design and prototyping which could then be leveraged by all academic institutions in the network.

3. **$50 million over 5 years ($10 million per year)** to support university access to industry-standard electronic design automation and technology computer aided design software tools, design flows, and multi-project wafer fabrication runs in semiconductor foundries for teaching and research purposes. Organizations similar to Metal Oxide Silicon Implementation Service, Muse Semiconductor or europractice-ic.com can serve as aggregators for the multi-project wafer runs and maintain the process design kits, libraries, and accompanying training material.

4. **$100 million over 5 years ($20 million per year)** to incentivize the hiring of at least 100 new faculty and teaching staff to ultimately increase the microelectronics output of the U.S. higher education system by 10,000 new graduates per year from across the education spectrum. This funding could be used to help cover the cost of salary and benefits for new faculty hires for the first 3 to 5 years, and to provide startup funds for new faculty hires. It should be noted that startup costs can easily exceed $1 million for university faculty who are experimentally oriented researchers.[35]

Recommendation 4: The Secretary of Commerce should ensure that NSTC-funded research (from Recommendation 8, below) supports on the order of 2,500 scholarships and research fellowships per year across the educational spectrum.

Because the high cost of post-secondary education can be a deterrent to student enrollment,[36,37] the Department of Commerce should ensure that NSTC-funded research supports on the order of 2,500 students each year through research fellowships (for graduate students) and scholarships (for undergraduate and community college students) to incentivize the pursuit and completion of degrees related to microelectronics. Some or all of these fellowships and scholarships could be offered in

[35] For example, the NSF Quantum Computing & Information Science (QCIS) Faculty Fellows program provided funding to cover the salary and benefits of new faculty hires in QCIS.

[36] Allen, D., & Wolniak, G. C. (2019). Exploring the effects of tuition increases on racial/ethnic diversity at public colleges and universities. *Research in Higher Education*, *60*(1), 18-43.

[37] Hemelt, S. W., & Marcotte, D. E. (2011). The impact of tuition increases on enrollment at public colleges and universities. *Educational Evaluation and Policy Analysis*, *33*(4), 435-457.

partnership with industry to guarantee jobs after graduation. NSF has existing selection and governance processes for granting scholarships and research fellowships that can be leveraged as appropriate for this NSTC-funded research.

Recommendation 5: The Department of Homeland Security should implement existing statutory and regulatory authorities to provide premium processing to newly filed Immigrant Petitions for employment-based second preference advanced degree immigrants seeking a National Interest Waiver to work in microelectronics endeavors.

While long-term educational investments are critical to developing the next generation of talent for the semiconductor industry, the United States must also enact policies to attract and retain the most talented, motivated, and highly educated individuals from around the world. Emblematic of the Biden administration's commitment to these types of policies, five such agency policies focused on international STEM talent recruitment and retention were enacted in January 2022.[38] One such policy update was to provide guidance detailing when advanced STEM degree holders can be considered to engage in endeavors of substantial merit that are in the national interest as part of immigrant petitions for a National Interest Waiver. This category is reserved for individuals who can self-petition because of the importance of their endeavor and their contribution to the endeavor. Ongoing efforts should continue in this vein, to assess whether further agency actions can be undertaken. For example, to ensure American companies have access to leading global talent, premium processing should be available upon initial filing of visa petitions for advanced degree experts working in microelectronics. In addition, legislation is needed to update the nation's governing immigration statute to reflect a variety of modern realities, including that country of origin should not matter when immigrants are selected based on their skills and education. While awaiting such comprehensive reform, an intermediate step is to award lawful permanent resident status for advanced STEM degree holders under current law without regard to per-country or worldwide numerical caps for individuals working in microelectronics endeavors.

Startups

A healthy startup ecosystem is vital for a thriving U.S. semiconductor industry. Indeed, today's leading semiconductor companies began as startups, from Intel and Advanced Micro Devices in the late 1960s to Qualcomm in the 1980s to NVIDIA and Broadcom in the early 1990s. Startups can be more agile than established companies and can target emerging markets and new technologies. Startups are good vehicles for taking R&D from universities and other research entities (e.g., DARPA) to market and are also excellent vehicles for spinning out important technology and products from established companies when they no longer fit in the company's strategic direction.

Despite the importance of startups, the rising costs of semiconductor development and the overall size of the semiconductor market have led to tremendous consolidation in the industry over the last

[38] On January 21, 2022, the Departments of Homeland Security and State announced five new international STEM talent policies, as summarized on this White House Fact Sheet. https://www.whitehouse.gov/briefing-room/statements-releases/2022/01/21/fact-sheet-biden-harris-administration-actions-to-attract-stem-talent-and-strengthen-our-economy-and-competitiveness

decade, from 160 companies in 2010 to 97 at the end of 2020.[39] Each year since 2013, semiconductor startups comprise less than one percent of venture capital investment (Figure 2).

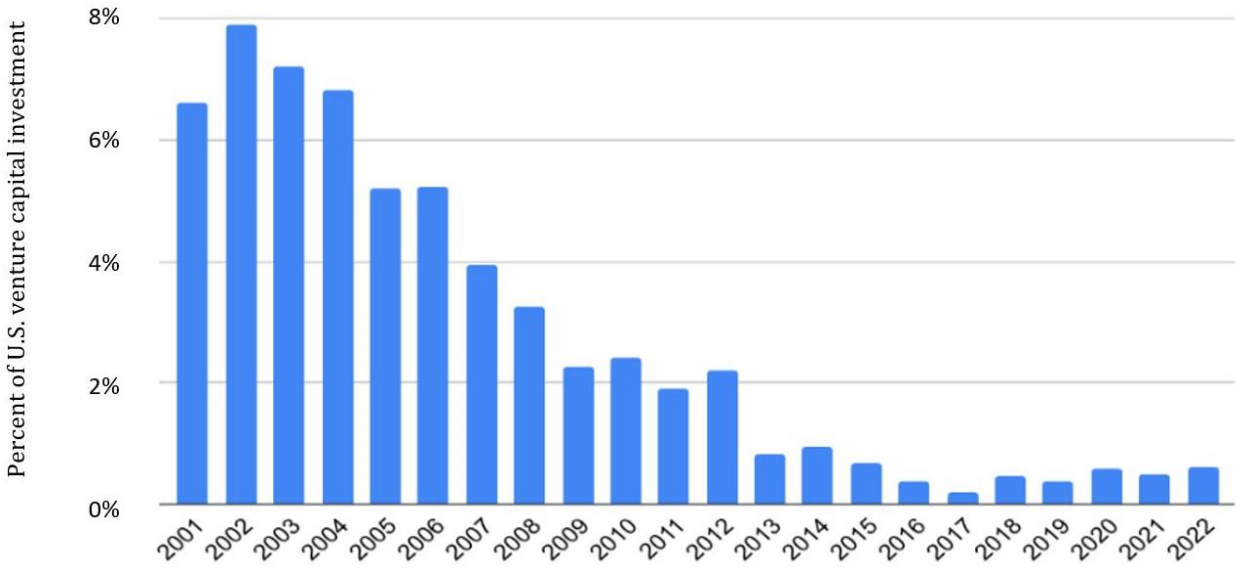

Figure 2: Percent of U.S. venture capital investment in semiconductors since 2001.
Source: Courtesy of Pear Ventures using original data retrieved from Crunchbase in August 2022.

Most venture capital organizations are drawn to startup technologies that require minimal investment and have the potential for a tenfold gain in 4-6 years.[40] Semiconductor startups, compared to software or services startups, require significantly more funding before going public or being acquired (tens to hundreds of millions of dollars), take longer to reach this stage, and have lower return on investment by orders of magnitude. For example, the investment needed ranges from tens of millions of dollars for simple analog, power, and sensing components to as much as $500 million for leading-edge semiconductors.[41] The high cost is largely due to design complexity, electronic design automation tools, IP licensing, tooling, and fabrication costs. This inhibits the creation of new companies and new products.

In the last few years, investment in semiconductor startups has increased due to the interest in artificial intelligence and new applications, from approximately 60 deals annually during the years

[39] Albert, G., & Alam, S. (2020, November 19) Semiconductor M&A; Are rising valuations worth it? *High Tech Perspectives, Accenture*. https://www.accenture.com/us-en/blogs/high-tech/semiconductor-valuation
[40] Zider, Bob, "How Venture Capital Works," *Harvard Business Review*, December 1998. https://hbr.org/1998/11/how-venture-capital-works
[41] Bauer, H., Burkacky, O., Lingemann, S., Pototzky, K., Kenevan, P., & Wiseman, B. (2020, August 20). *Semiconductor design and manufacturing: Achieving leading-edge capabilities.* McKinsey and Company. https://www.mckinsey.com/industries/advanced-electronics/our-insights/semiconductor-design-and-manufacturing-achieving-leading-edge-capabilities

2018-2020 to 75 deals in 2021.[42] However, these investments in semiconductors are far outweighed by those of China, which funded over 400 ventures in 2020.[43]

To help reduce the barriers to entry and encourage more startups in semiconductors, we recommend the following actions.

Recommendation 6: The Secretary of Commerce should ensure that by the end of 2023, the NSTC creates an investment fund on the order of $500 million to provide financial support and in-kind access to prototyping and tools for semiconductor startups.

An investment fund will offset the high capital requirements for semiconductor startups and the long time it takes them to reach positive cash flow. This will level the playing field, making these investments more attractive and hence facilitating the creation of more semiconductor startups and supporting and accelerating innovation in the semiconductor ecosystem. The NSTC investment fund could directly invest in semiconductor startups or semiconductor incubators, which would provide industry expertise, nurturing and guidance, as well as financial support. The NSTC investment fund would have the highest impact through investing in early-stage companies in the pre-seed and seed rounds which are typically the highest risk. The NSTC should also reserve capacity to provide in-kind support to qualified startups with reduced or zero cost access to prototyping and tools.

Recommendation 7: The Secretary of Commerce should ensure that the NSTC creates or funds the creation of a "chiplet"[44] platform with a complete software stack by the end of 2025 so that startups and academic institutions can integrate their custom chiplet(s) with the NSTC-supported chiplet platform to demonstrate new innovations with dramatically reduced investment and time.

Much of semiconductor design complexity can be found in the non-innovative part of the product (especially true of leading-edge systems-on-a-chip). The challenge for many startups and academic institutions is that they must acquire and integrate several critical IP components from microprocessors to high-speed interfaces to custom memories, which are just the basic components required for a working system before they can add their innovative "secret sauce."

Software development often avoids a similar challenge by adding a small or modest amount of code onto a complex, but existing and working codebase. We can do the same for chip design by building a "chiplet" ecosystem—which would allow small/modest but innovative hardware and code to be added to an already working hardware/software platform to capture the impact of the innovation quickly and cheaply. To do this, a platform system-on-a-chip must be made available, with a supporting software stack, that provides an interface to which small "chiplets" containing the innovative part of the system can be attached using advanced packaging. Such an ecosystem would enable a startup or academic institution to design just the innovative part of the system (hardware and software) while substantially lowering their development costs and required investments. This

[42] Restagno, J. (2022, February 8). Shortage of chips; no shortage of capital. *Silicon Valley Bank*. https://www.svb.com/industry-insights/hardware-frontier-technology/shortages-drive-record-investment-in-semiconductor-startups

[43] Sheng, W. (2021, March 4). Where China is investing in semiconductors, in charts. *Technode*. https://technode.com/2021/03/04/where-china-is-investing-in-semiconductors-in-charts

[44] A chiplet platform is an integrated circuit that is composed of multiple smaller chips where the common, non-innovative parts of a product have been specifically designed so that customizable components ("chiplets") can be added to address particular applications, performance, or functionality.

would be analogous to how Apple's App Store and Google Play changed software design and delivery, allowing many more people to create and sell their programs faster, simpler, and with less overhead.

We expect that creating a chiplet ecosystem—with software—will reduce the capital required for a system-on-a-chip startup by an order of magnitude and reduce the time required to get a product to market by a factor of two or more. Reducing these barriers, in turn, will result in far more opportunities for semiconductor startups to develop products and also enable academic innovation to be simpler, faster, and cheaper.

The NSTC should build upon existing programs where relevant for this "chiplet" ecosystem, including efforts that are underway at DARPA as part of the Electronics Research Initiative[45] and other industry efforts.[46]

National Research Agenda and Grand Challenges

U.S. leadership in the global semiconductor ecosystem requires significant and sustained advancements across multiple critical interrelated technical areas. Within each area, there are numerous technical challenges that require both fundamental research and prototyping capabilities to shepherd new solutions from research prototypes through scaleup and commercial adoption.

Recommendation 8: The Secretary of Commerce should ensure that the NSTC founding charter allocates a significant portion of the annual funding, on the order of 30 to 50 percent, to directly fund a national research agenda. The research agenda should be broad in nature and address the following areas: materials, process, and manufacturing technologies; packaging and interconnect technologies; energy-efficient computing and domain-specific accelerators; design automation tools and methods; semiconductor and system security; and semiconductors and life sciences.

Although a large portion of the funding of the NSTC will be used for much-needed equipment and infrastructure, we believe a significant portion of the funding should also be used to directly fund research and collaboration. A broad and robust research agenda is critical to the success of the NSTC and U.S. global competitiveness.

Below we identify some of the key research themes that would be highly impactful to address as part of the NSTC research agenda. The final research agenda should be proposed by the NSTC Executive Team guided by the NSTC Technology Advisory Council.

(a) Materials, Process, and Manufacturing Technologies

Moore's law, which is the observation that the number of transistors on an integrated circuit doubles every two years, thereby increasing performance, has governed the semiconductor industry for more than 50 years. However, this trend has slowed down in recent years, and fundamental physical challenges impede continued reductions in transistor dimensions and improvement in performance. Innovation is required in next generation materials, process technologies, and high-volume

[45] Keeler, G. (n.d.). *Common Heterogeneous Integration and IP Reuse Strategies (CHIPS)*. DARPA. https://www.darpa.mil/program/common-heterogeneous-integration-and-ip-reuse-strategies
[46] *Universal Chiplet Interconnect Express*. (2022). https://www.uciexpress.org

manufacturing solutions to continue to reduce chip dimensions and make the needed advances in performance, energy efficiency, and cost.

The NSTC research agenda should encompass materials, process, and manufacturing technologies required to enable advanced logic, advanced memory, analog, mixed-signal and RF devices which are all essential to building full systems. In addition, foundational process technologies for heterogeneous integration (i.e., mixing different technologies on the same chip) and 3D stacking (i.e., stacking chips on top of each other to create denser and more capable chips) are critical.

To ensure a fast ramp from initial ideas in a laboratory to high-volume manufacturing, materials and equipment should be developed in tandem with the devices and process technologies. These activities would be carried out primarily in the advanced logic, advanced memory, and analog and mixed-signal COEs.

(b) Packaging and Interconnect Technologies

Packaging and interconnect technologies have become even more important to continue performance, density, and system-level improvements in recent years as traditional techniques for reducing the dimensions of chips have slowed down. This requires innovation and co-development at the silicon, package, design, architecture, and system levels. The packaging COE with funding from the NAPMP is a critical resource to both advance research in this area and provide prototyping capabilities.

Cost-effective wafer bonding techniques, advanced modeling capabilities, and efficient power delivery systems to enable heterogeneous integration and 3D stacking solutions need to be developed across a wide variety of process technologies. Establishment of industry standard interfaces which can connect logic, memory, and analog components in chiplet ecosystems should also be addressed.

The advanced package and interconnect technologies must also provide secure plug-and-play technologies and standards to allow seamless integration of a variety of semiconductor components, which is critical for future U.S. semiconductor technology and supply chain strength.

(c) Energy-Efficient Computing and Domain-Specific Accelerators

Domain-specific accelerators, i.e., specialized chips that are focused on specific applications, have the potential to continue scaling of performance and energy efficiency as semiconductor technology scaling slows, and they are critical to achieving the grand challenges described in Recommendation 9. One challenge in this area is to investigate domain-specific accelerator architectures and design methodologies that are more resilient to fast-paced changes in algorithms and applications. The resilience can come from introducing programmability that is targeted for a domain. Such accelerators can propel progress in several domains of interest, including artificial intelligence and machine learning (inference and training in the cloud and at the edge), graph analytics, security, communications, bioinformatics, and continuous and discrete optimization. In addition, research is needed on standardizing the interface between the accelerator and the processor, memory system, and the rest of the system-on-a-chip.

Hardware specialization for domains typically entails significant modifications to the software stack to properly leverage the accelerators. Because of the large overhead of maintaining the entire software stack, real-world usage of an accelerator lags far behind its design. A key challenge, therefore, is to automate the co-design of programmable accelerators and the compilers that map applications to them, for fast-changing application domains. We recommend investments that could enable a comprehensive software ecosystem to make writing and executing new applications efficient and accessible for a wide range of accelerators.

(d) Design Automation Tools and Methodologies

Innovation in design automation tools and methodologies are critical to reduce time to market and achieve new levels of performance and system integration. Raising the level of design so that chips and IPs can be compiled from high-level descriptions (above register-transfer level) much as software is compiled has the potential to greatly increase design productivity. Artificial intelligence can be applied to every step of the design process to both increase productivity and improve the quality of results. Design tools, some based on artificial intelligence, can greatly increase the productivity of analog, mixed-signal, and RF circuits which are largely designed by hand today.

In addition, emulation and virtual prototyping technology that supports the verification of the exponentially growing complexity of both hardware and software is required for next-generation heterogeneous architectures.

(e) Semiconductors and System Security

Criminal and state-sponsored cyber-attacks pose increasing threats to the United States. To enable the implementation of secure systems, every aspect of the system must be considered including sensors, data converters, computing, memory, storage, and communications, while providing robustness against side-channel attacks and ensuring security of supply chains. There is a tremendous opportunity for the design of secure semiconductor chips. To maximize effectiveness, security must be pursued as an integral part of design, not as an add-on after the chip is designed.

Academia, industry and government stakeholders have an opportunity to standardize a trusted approach for systems implementation. The specific opportunity is to bring together algorithm and software/systems designers with chip designers in a center of excellence, to develop the next generation of secure systems. Although open-source security approaches are the best for innovation and transparency, they remain unpalatable for the industry. We must address this reluctance in a way that enables the United States to continue to be the global leader in standardized security approaches.

We envision a research agenda in this area that should include, but is not limited to, the following: (1) design for fully secure end-to-end hardware and software solutions that are secure against various forms of attacks on operation, data, and communications; (2) security in the chip design tool chain that would enable end-to-end security solutions to be verified by design; (3) secure hardware supply chain covering chip fabrication, packaging, and system integration; (4) implementation of post-quantum cryptography; (5) implementation of low-power cryptography for secure communications and transactions; and (6) other privacy preserving hardware implementations for processing encrypted data.

(f) Semiconductors and Life Sciences

There are many deployed examples of semiconductors having a positive impact on human health, from wearable cardiac monitors, glucose sensors, medical robots, and ultrasound imaging to implantable devices such as pacemakers and deep brain stimulators. The COVID-19 pandemic has shown that innovations in life sciences can happen at unprecedented speed, from producing rapid testing technologies to breakthrough mRNA-based vaccines. Semiconductors have the potential to play a central role in the early detection and prevention of diseases, continuous monitoring, and therapies. The United States is a global leader in life sciences R&D and some of those initiatives are already leveraging the potential of microelectronics to advance neuroscience and biomedical research.[47] We believe that this can be even further accelerated given the tremendous capabilities of machine learning, heterogeneous integration, and improvements in performance and size of devices. Some example research directions include, but are not limited to, the following: (1) multi-modal neuroscience solutions that can enable the monitoring, mitigation, or cure of various diseases; (2) implantable and ingestible electronics; (3) interfacing semiconductors to biology for specific sensing functions; and (4) next-generation wearable bio sensors and actuators.

These systems will need to integrate diverse technologies, such as sensors based on a variety of materials and even biological cells, embedded machine learning and other processing, memory, secure communications, and actuators, and materials that can function well in harsh environments (e.g., inside the human body). Since the systems must operate from tiny energy sources or even operate from energy harvesting, there is a critical need to develop ultra-low-power solutions.

Materials experimentation is key, but traditional semiconductor fabs are not set up appropriately to introduce the non-standard or "dirty materials" needed for life sciences. Access to advanced packaging with the ability to introduce new materials for harsh environments is also needed. The NSTC COEs can provide access to these critical prototyping facilities and packaging solutions.

Finally, access to large, anonymized datasets to train machine learning models would accelerate research in these areas as well as help to navigate the slow approval processes for new hardware solutions for life sciences. The NSTC COE should work with government agencies, universities, medical centers, and health technology, semiconductor, and insurance companies to improve access to large datasets for researchers.

Recommendation 9: The NSTC should identify a set of nationwide grand challenges that are enabled through collaboration across the NSTC industrial membership and NSTC-funded research. These grand challenges should span three complementary areas that would benefit from large-scale nationwide collaboration: advanced computing into the zettascale era; significantly reducing design complexity; and proliferating semiconductors in life sciences applications.

For future large-scale innovation, broad and deep collaboration is needed at the process, device, architecture, design, applications, and system levels. The NSTC is well suited to drive large-scale and nationwide collaboration across NSTC-funded research teams, NSTC industrial members, startups, and government to drive step-function improvements in capabilities. We recommend the NSTC

[47] Examples of existing initiatives include the BRAIN (https://braininitiative.nih.gov) and SPARC programs (https://commonfund.nih.gov/sparc).

allocate a portion of the research funding defined in Recommendation 8 towards several large-scale projects that become nationwide grand challenges. These grand challenges would set out ambitious goals that target significant increases in performance and/or capability in the 5- to 10-year time horizon. We recommend that these grand challenges span the following topics:

a) **Advanced Computing into the Zettascale Era:** The United States should be the first to build a "zettascale" supercomputer, with the goal of being 1,000 times faster than the fastest supercomputer that is available today at one-hundredth the energy per operation of systems available today.[48] This incredible amount of computing capacity would enable extremely complex calculations to be accomplished at a different scale and efficiency than what can be accomplished today and will unleash a new wave of scientific discoveries in such areas as predicting climate change, understanding and predicting wildfire activity, designing vaccines, personalizing cancer treatment, understanding the human brain, and much more. In addition, this massive increase in efficient computing capability could enable next-generation experiences such as the metaverse and new forms of sensory interaction across the internet. Achieving these objectives would require revolutionary advances in logic, memory, mixed-signal, and packaging technologies, and thus would require interdisciplinary research between the NSTC COEs.

b) **Reducing Design Complexity:** Create platforms, methodologies, and tools to reduce design complexity and enable chips to be built using one-tenth the person-hours that are required today. Semiconductor design costs and complexity have increased significantly, due to technology scaling/integration and ever more demanding requirements for power, performance, area, manufacturability, reliability, and security. These issues are further compounded by shortfalls in the workforce. Advancements in design tools and methodologies can both boost workforce productivity and lower barriers to entry for startups, encouraging a larger and more diverse pool of participants in the U.S. semiconductor industry.

c) **Semiconductors in Life Sciences**: Create an energy-efficient, scalable, and secure platform architecture for monitoring and treatment of health, wellness, and disease. The platform should be seamless and minimally invasive, assisting patients and doctors in sensing, actuation, monitoring, mitigating symptoms, and treating various conditions. Creating a library of such tools will allow advances well beyond what is possible today. To drive the most impactful applications, significant improvements in sensing, computing, and communications are required. For example, today's neural probes can record electrical signals from thousands of sites and they collect data from hundreds to thousands of neurons. The goal is to increase the number of neurons from which signals can be recorded by a factor of 100 to 1,000. Similarly, there is the need to collect a large amount of data from the body as well as the need for this data to be kept private, which will require creating a set of ultra-low power security solutions at one-hundredth the energy consumption of today's solutions.

U.S. Government Coordination and Metrics

Federal government investments in semiconductors span the Department of Commerce, Department of Energy, Department of Defense, NSF, Department of Health and Human Services, and other agencies. The U.S. government has made and is committed to making significant investments to

[48] Oak Ridge National Laboratory (2022, May 30). *Frontier supercomputer debuts as world's fastest, breaking exascale barrier*. https://www.ornl.gov/news/frontier-supercomputer-debuts-worlds-fastest-breaking-exascale-barrier

revitalize the U.S. semiconductor ecosystem, with a variety of initiatives to meet that goal. Effective coordination of such initiatives is essential to reduce duplication of effort and maximize the use of and return on taxpayer dollars. Therefore, the United States should develop a cohesive national strategy that accelerates progress toward a strong, world-leading semiconductor industry.

Recommendation 10: To improve visibility into federal semiconductor investment efforts, measure the progress across the industry at the federal level, and maximize the leverage of such investments, we recommend the following:

a) **Starting in 2023, and annually thereafter, the Networking and Information Technology Research and Development (NITRD) program should collate and publish annual investment figures for semiconductors across all federal agencies.**

b) **The NSTC should encourage all agencies with semiconductor R&D investments to leverage and utilize the NSTC facilities and capabilities. We recommend the NSTC expand and co-fund programs with other agencies and in public-private partnership where the research agendas are synergistic including, for example, DARPA's Electronics Resurgence Initiative, Research on the Future of Semiconductors sponsored by the Computer and Information Science and Engineering Directorate at NSF, and the broad multi-sector collaborations enabled by the Semiconductor Research Corporation.**

c) **The Secretary of Commerce should develop and regularly evaluate performance measures to assess progress, effectiveness, outcomes, and impact of the CHIPS and Science Act initiatives and report them annually to the President.**

Potential metrics for the NSTC could include but not be limited to:

- Annual review of performance and schedule of NSTC COE and project milestones, and progress towards the grand challenge objectives
- Revenue per year from non-federal memberships (includes in-kind contributions)
- Number of patents and copyrights submitted and granted
- Number of organizations (startups, university, industry) using NSTC facilities for prototyping
- Number of semiconductor startups funded with direct or in-kind NSTC contributions
- Number of university engagements:
    - Number of students sponsored
    - Number of papers published on NSTC-based research
    - Number of students aided by the workforce development funding
- Economic value to the United States as measured by:
    - Technology leadership position
    - U.S. semiconductor supply chain robustness
    - Direct and indirect jobs supported and created
    - National security enabled via semiconductors

This list of metrics is by no means fully comprehensive; however, it is very important that metrics of success by phase of investment are defined very early in the establishment of the NSTC to ensure clear, universally understood objectives.

Conclusion

We are living in a defining moment for American semiconductor innovation and international competitiveness. The bipartisan passage of the CHIPS and Science Act has provided a once-in-a-generation opportunity to reassert our global leadership in this key technology that is vital to nearly every aspect of modern life. Implementation of these 10 recommendations will lay a strong foundation on which to revitalize the U.S. semiconductor R&D ecosystem, significantly accelerating innovation and enhancing our economic competitiveness in this critical field for the next generation.

Acknowledgements

The members of PCAST wish to thank the staff in the Office of Science and Technology Policy (OSTP) for their various contributions throughout the preparation of this report. PCAST would especially like to thank Alondra Nelson, Deputy Assistant to the President and Performing the Duties of Director of the White House Office of Science and Technology Policy. PCAST also expresses its gratitude to Marc Aidinoff, Kei Koizumi, Asad Ramzanali, and Ellen Qualls in OSTP. Staff of the Science and Technology Policy Institute, which is managed by the Institute for Defense Analyses, provided skillful support to PCAST. We especially acknowledge Emily Grumbling, Brian Zuckerman, and Keith Crane. Finally, we wish to express a heartfelt thanks to the staff at the Department of Energy, particularly Karen Talamini, who have worked tirelessly in administering PCAST.

Appendix A. External Experts Consulted

PCAST sought input from a diverse group of additional experts and stakeholders. PCAST expresses its gratitude to those listed here who shared their expertise. They did not review drafts of the report, and their willingness to engage with PCAST on specific points does not imply endorsement of the views expressed herein. Responsibility for the opinions, findings, and recommendations in this report and for any errors of fact or interpretation rests solely with PCAST.

Jeff Alstott
Assistant Director for Technology Competition and Risks
Office of Science and Technology Policy
The White House

Polina Anikeeva
Professor of Materials Science and Engineering
Professor of Brain and Cognitive Sciences
Massachusetts Institute of Technology

Aart de Geus
Chairman and Co-CEO
Synopsys Inc.

Lisa Friedersdorf
Former Director
National Nanotechnology Coordination Office
Office of Science and Technology Policy
The White House

Pat Gelsinger
CEO
Intel

Mar Henderson
Founding Managing Partner
Pear Ventures

Saif Khan
Director of Technology and National Security
National Security Council
The White House

Doug Kirkpatrick
CEO
Eridan Communications

Rodrigo Liang
CEO and Co-founder
SambaNova Systems

Jason Matheny
Former Deputy Director for National Security
Office of Science and Technology Policy
The White House

Carl McCants
Special Assistant to the Director
DARPA

Rikky Muller
Associate Professor of Electrical Engineering and Computer Sciences
University of California, Berkeley

John Neuffer
President and CEO
Semiconductor Industry Association

Amy Nice
Assistant Director for International Science and Technology Workforce
Office of Science and Technology Policy
The White House

David Z. Pan
Silicon Laboratories Endowed Chair in Electrical Engineering
The University of Texas at Austin

Sreenivas Ramaswamy
Senior Policy Advisor
Department of Commerce

Doug Rand
Senior Advisor to the Director
U.S. Citizenship and Immigration Services
Department of Homeland Security

Wally Rhines
President and CEO
Cornami, Inc.

Kamie Roberts
Director
National Coordination Office
Networking and Information Technology Research and Development (NITRD) Program
Office of Science and Technology Policy
The White House

Mark Rosker
Director of Microsystems Technology Office
DARPA

Devanand K. Shenoy
Principal Director for Microelectronics
Director of Defense Microelectronics Cross-Functional Team
Office of the Under Secretary of Defense for Research and Engineering
Department of Defense

Dawn Song
Professor of Computer Science
University of California, Berkeley

Reed Sturtevant
General Partner
The Engine

Lip-Bu Tan
Chairman
Walden International
Executive Chairman
Cadence Design Systems

Vinod Vaikuntanathan
Professor of Computer Science
Massachusetts Institute of Technology

Luc Van den hove
President and CEO
IMEC

Naveen Verma
Professor of Electrical and Computer Engineering
Director of Keller Center for Innovation in Engineering Education
Princeton University

Lloyd Whitman
Former Assistant to the Director for Science Policy and Planning
NSF